

April 1995

LM1893/LM2893 Carrier-Current Transceiver†

General Description

Carrier-current systems use the power mains to transfer information between remote locations. This bipolar carrier-current chip performs as a power line interface for half-duplex (bi-directional) communication of serial bit streams of virtually any coding. In transmission, a sinusoidal carrier is FSK modulated and impressed on most any power line via a rugged on-chip driver. In reception, a PLL-based demodulator and impulse noise filter combine to give maximum range. A complete system may consist of the LM1893, a COPS™ controller, and discrete components.

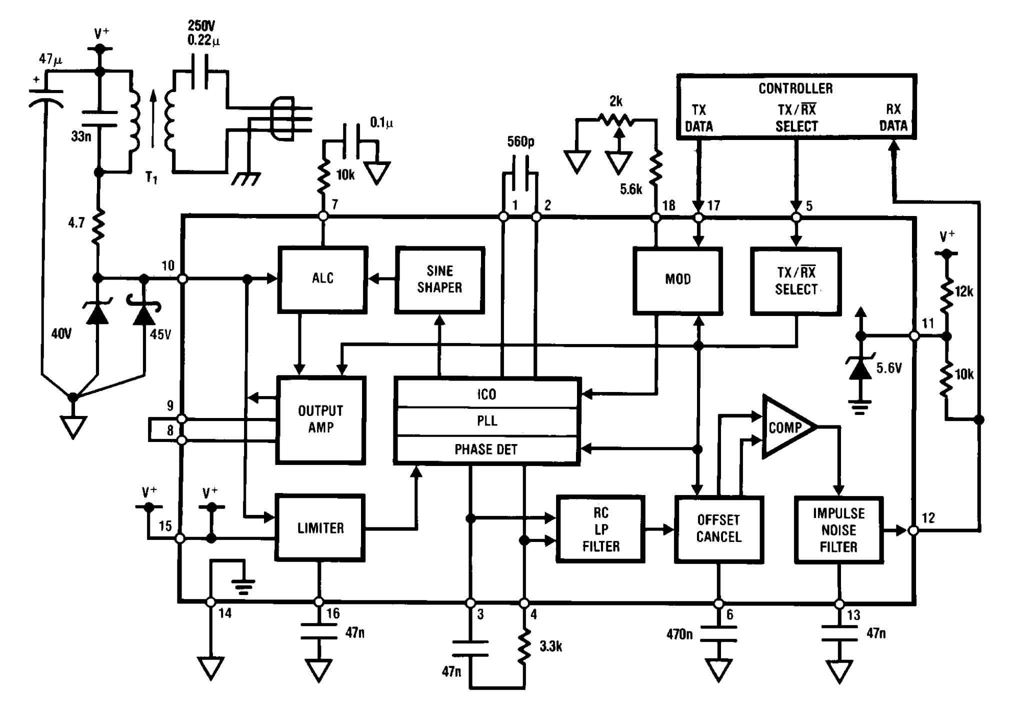
Features

- Noise resistant FSK modulation
- User-selected impulse noise filtering
- Up to 4.8 kBaud data transmission rate
- Strings of 0's or 1's in data allowed
- Sinusoidal line drive for low RFI
- Output power easily boosted 10-fold
- 50 to 300 kHz carrier frequency choice
- TTL and MOS compatible digital levels
- Regulated voltage to power logic
- Drives all conventional power lines

Applications

- Energy management systems
- Home convenience control
- Inter-office communication
- Appliance control
- Fire alarm systems
- Security systems
- Telemetry
- Computer terminal interface

Typical Application



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FIGURE 1. Block diagram of carrier—current chip with a complement of discrete components making a complete $F_O = 125$ kHz, $f_{DATA} = 360$ Baud transceiver. Use caution with this circuit—dangerous line voltage is present.

BI-LINE™ and COPS™ are trademarks of National Semiconductor Corp.

†Carrier-Current Transceivers are also called Power Line Carrier (PLC) transceivers.

RRD-B30M115/Printed in U. S. A.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply voltage		30 V
Voltage on pin 12		55 V
Voltage on pin 10 (Note 1)		41 V
Voltage on pins 5 and 17		40 V
5.6 V DC zener current		100 mA
Junction temperature:	transmit mode	150°C
	receive mode	125°C
Electro-Static Discharge (120 pF, 1500Ω)		1KV
Maximum continuous dissipation, $T_A = 25°C$,		
plastic DIP N (Note 2):	transmit mode	1.66 W
	receive mode	1.33 W
Operating ambient temp. range		−40 to 85°C
Storage temperature range		−65 to 150°C
Lead temp., soldering, 7 seconds		260°C

Note: *Absolute maximum ratings indicate limits beyond which damage to the device may occur. Electrical specifications are not ensured when operating the device above guaranteed limits but below absolute maximum limits, but there will be no device degradation.*

General Electrical Characteristics

(Note 3). The test conditions are: $V^+ = 18V$ and $F_O = 125$ kHz, unless otherwise noted.

#	Parameter	Conditions	Typical	Test Limit (Note 4)	Design Limit (Note 5)	Limit Units
1	5.6 V Zener voltage, V_Z	Pin 11, $I_Z = 2$ mA	5.6	5.2 5.9		V min. V max.
2	5.6 V Zener resistance, R_Z	Pin 11, $R_Z = (V_Z@10\text{ mA} - V_Z@1\text{ mA})/(10\text{ mA} - 1\text{ mA})$	5			Ω
3	Carrier I/O peak survivable transient voltage, V_{OT}	Pin 10, discharge 1 μF cap. charged to V_{OT} thru < 1Ω	80	60		V max.
4	Carrier I/O clamp voltage, V_{OC}	Pin 10, $I_{OC} = 10$ mA, RX mode 2N2222 diode pin 8 to 9	44	41 50		V min. V max.
5	Carrier I/O clamp resistance, R_{10}	Pin 10, $I_{OC} = 10$ mA	20			Ω
6	TX/$\overline{RX}$ low input voltage, V_{IL}	Pin 5	1.8	0.8		V max.
7	TX/$\overline{RX}$ high input voltage, V_{IH}	Pin 5 (Note 9)	2.2	2.8		V min.
8	TX/$\overline{RX}$ low input current, I_{IL}	Pin 5 at 0.8 V	−2	−20 1		μA min. μA max.
9	TX/$\overline{RX}$ high input current, I_{IH}	Pin 5 at 40 V	10^{-4}	−1 10	**0**	μA min. μA max.
10	RX−TX switch-over time, T_{RT}	Time to develop 63% of full current drive thru pin 10	10			μs
11	TX−RX switch-over time, T_{TR}	1 bit time, $T_B = 1/(2F_{DATA})$. Time T_{TR} is user controlled with C_M, see Apps. Info.	2			bit
12	ICO initial accuracy of F_O	TX mode, $R_O = 6.65$ kΩ, $C_O = 560$ pF $F_0 = (F_1 + F_2)/2$	125	113 137		kHz min. kHz max.
13	ICO temperature coefficient of F_O	TX or RX mode, $(F_{OMAX} - F_{OMIN})/(T_{JMAX} - T_{JMIN})$	**−100**			PPM/°C
14	Temperature drift of F_O	TX or RX mode, $-40 \leq T_J \leq T_{JMAX}$	**±2.0**		**±5.0**	% max.

Transmitter Electrical Characteristics

(Note 3). The test conditions are: $V^+ = 18$ V and $F_O = 125$ kHz unless otherwise noted. The transmit center frequency is F_O, FSK low is F_1, and FSK high is F_2.

#	Parameter	Conditions	Typical	Test Limit (Note 4)	Design Limit (Note 5)	Limit Units
15	Supply voltage, V^+, range	Meets test 17 spec. at $T_J = 25°C$ and: $\lvert(F_1[14V] - F_1[18V])/F_1[18V]\rvert < 0.01$ $\lvert(F_1[24V] - F_1[18V])/F_1[18V]\rvert < 0.01$	**13** **40**	14 24	**15** **23**	V min. V max.
16	Total supply current, I_{QT}	Pin 15. Pin 12 high. I_{QT} is I_Q through pin 15 and the average current I_{ODC} of the Carrier I/O through pin 10	52	79		mA max.
17	Carrier I/O output current, I_O	100Ω load on pin 10	70	45		mApp min.
18	Carrier I/O lower swing limit, V_{ALC}	Pin 10. Set internally be ALC. 2N2222 diode pin 8 to 9	4.7	4.0 5.7		V min. V max.
19	THD of I_O (Note 6)	Q of 10 tank driving 10Ω line 100Ω load, no tank	0.6 5.5		**5.0** 9	% max. % max.
20	FSK deviation, $F_2 - F_1$	$(F_2 - F_1)/([F_2 + F_1]/2)$	4.4	3.7 5.2		% min. % max.
21	Data In. low input voltage, V_{IL}	Pin 17	1.7	0.8		V max.
22	Data In. high input voltage, V_{IH}	Pin 17 (Note 9)	2.1	2.8		V min.
23	Data In. low input current, I_{IL}	Pin 17 at 0.8 V	−1	−10 1		μA min. μA max.
24	Data In. high input current, I_{IH}	Pin 17 at 40 V	10^{-4}	−1 10	**0**	μA min. μA max.

Receiver Electrical Characteristics (Note 3). The test conditions are: $V^+ = 18$ V, $F_O = 125$ kHz, ±2.2% deviation FSK, $F_{DATA} = 2.4$ kHz, $V_{IN} = 100$ mVpp, in the receive mode, unless otherwise noted.

#	Parameter	Conditions	Typical	Test Limit (Note 4)	Design Limit (Note 5)	Limit Units
25	Supply voltage, V^+, range	Functional receiver (Note 7)	**12** **37**	13 30	**13.5** **28**	V min. V max.
26	Supply current, I_{QT}	I_{QT} is pin 15 (V^+) plus pin 10 (Carrier I/O) current. 2.4 kΩ Pin 13 to GND.	11	5 14		mA min. mA max.
27	Carrier I/O input resistance, R_{10}	Pin 10	19.5	14 30		kΩ min. kΩ max.
28	Max. data rate, F_{MD}	Functional receiver (Note 7), C_F = 100 pF, R_F = 0Ω, no tank, 2.4 kHz = 4.8 kBaud	10	4.8	**2.4**	kBaud
29	PLL capture range, F_C	C_F = 100 pF, R_F = 0 Ω	±40	±15	±**10**	% min.
30	PLL lock range, F_L	C_F = 100 pF, R_F = 0 Ω	±45	±15		% min.
31	Receiver input sensitivity, S_{IN}	For a functional receiver (Note 8) Referred to chip side (pin 10) of the line-coupling XFMR: F_O = 50 kHz F_O = 300 kHz Referred to line side of XFMR: (assuming a 7.07:1 XFMR) F_O = 50 kHz F_O = 300 kHz	1.8 2.0 1.4 0.26 0.29 0.20	10	**12**	mV_{RMS} mV_{RMS} mV_{RMS} mV_{RMS} mV_{RMS} mV_{RMS}
32	Tolerable input dc voltage offset range, V_{INDC}	Pin 10 lower than pin 15 by V_{INDC}	2	0.1		V max.
33	Data Out. breakdown voltage	Pin 12, leakage I ≤ 20 μA	70	55		V min.
34	Data Out. low output, V_{OL}	Pin 12, sat. voltage at I_{OL} = 2 mA	0.15	0.4		V max.
35	Impulse noise filter current, I_I	Pin 13 charge and discharge current	±55	±45 ±85		μA min. μA max.
36	Offset hold cap. bias voltage, V_{CM}	Pin 6	2.0	1.3 3.5		V min. V max.
37	Offset hold capacitor max. drive current, I_{MCM}	Pin 6. V(pin 3) − V(pin 4) = ±250 mV	±55	±25 ±80		μA min. μA max.
38	Offset hold bias current, I_{OHB}	Pin 6, TX mode. Bias pin 6 as it self-biased during test 31.	−0.5	−20	**−40** **40**	nA min. nA max.
39	Phase comparator current, I_{PC}	Bias pins 3 and 4 at 8.5 V I_{PC} = I(pin 3) + I(pin 4), TX mode	100	50 200		μA min. μA max.
40	Phase detector output resistance, R_{PD}	Pins 3 and 4. R_{PD} = (V@100μA − V@50μA)/(50μA)	10	6 18		kΩ min. kΩ max.
41	Phase detector demodulated output voltage, V_{PD}	Pin 3 to 4, measured after filtering out the $2F_O$ component	100	60 180		mVpp min. mVpp max.
42	Fast offset cancel voltage "window" -to-V_{PD} ratio, V_W/V_{PD}	$V_{PIN3} - V_{PIN4} = \pm V_{WINDOW}$ + DC offset Drive for ±1 μA pin 6 current	0.95	0.70 1.20		V/V min. V/V max.
43	Power supply rejection, PSRR	C_L = 0.1 μF. PSRR = CMRR. 120 Hz	80			dB min.

Note 1: More accurately, the maximum voltage allowed on pin 10 is V_{OC}, and V_{OC} ranges from 41 to 50V. Also, transients may reach above 60V; see the transient peak voltage characteristic curve.

Note 2: The maximum power dissipation rating should be derated for device operation above 25°C to insure that the junction temperature remains below the maximum rating. Use a θ_{JA} of 75°C/W for the N package using a socket in still air (which is the worst case). Consult the Application Information section for more detail.

Note 3: The **boldface** values apply over the full junction temperature range for the specified supply voltage range. All other numbers apply at $T_A = T_J = 25°C$. Pin numbers refer to LM1893. LM2893 tested by shorting Carrier In to Carrier Out and testing it as an LM1893.

Note 4: Guaranteed and 100% production tested.

Note 5: Guaranteed (but not 100% production tested) over the temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Note 6: Total harmonic distortion is measured using THD = [I_{RMS} (all components at or above $2F_O$)]/[I_{RMS} (fundamental)].

Note 7: Receiver function is defined as the error-free passage of 1 cycle of 50% duty-cycle 2.4 kHz square-wave data (2 sequential 208 μS bits), with the first bit being a "1." All of the data transitions (edges) must fall within ±10% (±20.8 μs) of their noise-free positions. RX time delay is minimized by using no impulse noise filter cap. C_I for this test.

Note 8: During the sensitivity check, note 7 requirements are followed with these exceptions: (1) data rate F_{DATA} = 1.2 kHz, (2) all of the data transitions must fall within ±20% (±41.6 μs) of their noise-free positions, and (3), a time-domain filter capacitor (C_I) is used. The time delay of C_I is ½ bit, or 208 μs. (C_I is approximately 6200 pF).

Note 9: For TTL compatibility use a pull-up resistor to increase min. V_{OH} to above 2.8 V.

Typical Performance Characteristics ($V^+ = 18V$, $F_O = 125$ kHz, circuit of *Figure 1*, pin numbers for LM1893)

Total Current Consumption, I_{QT}, vs Supply Voltage

Total Current Consumption, I_{QT}, vs Junction Temperature

Chip Bias Current, i_Q, vs Supply Voltage

Chip Bias Current, I_Q, vs Junction Tempurature

Output Stage DC Current, I_{ODC}, vs Output Voltage

Output Stage DC Current, I_{ODC}, vs Junction Temperature

Transient Voltage Survival vs Pulse Time

Transmitter AC Output Current vs Junction Temperature

Transmitter Sinusoid THD vs Junction Temperature

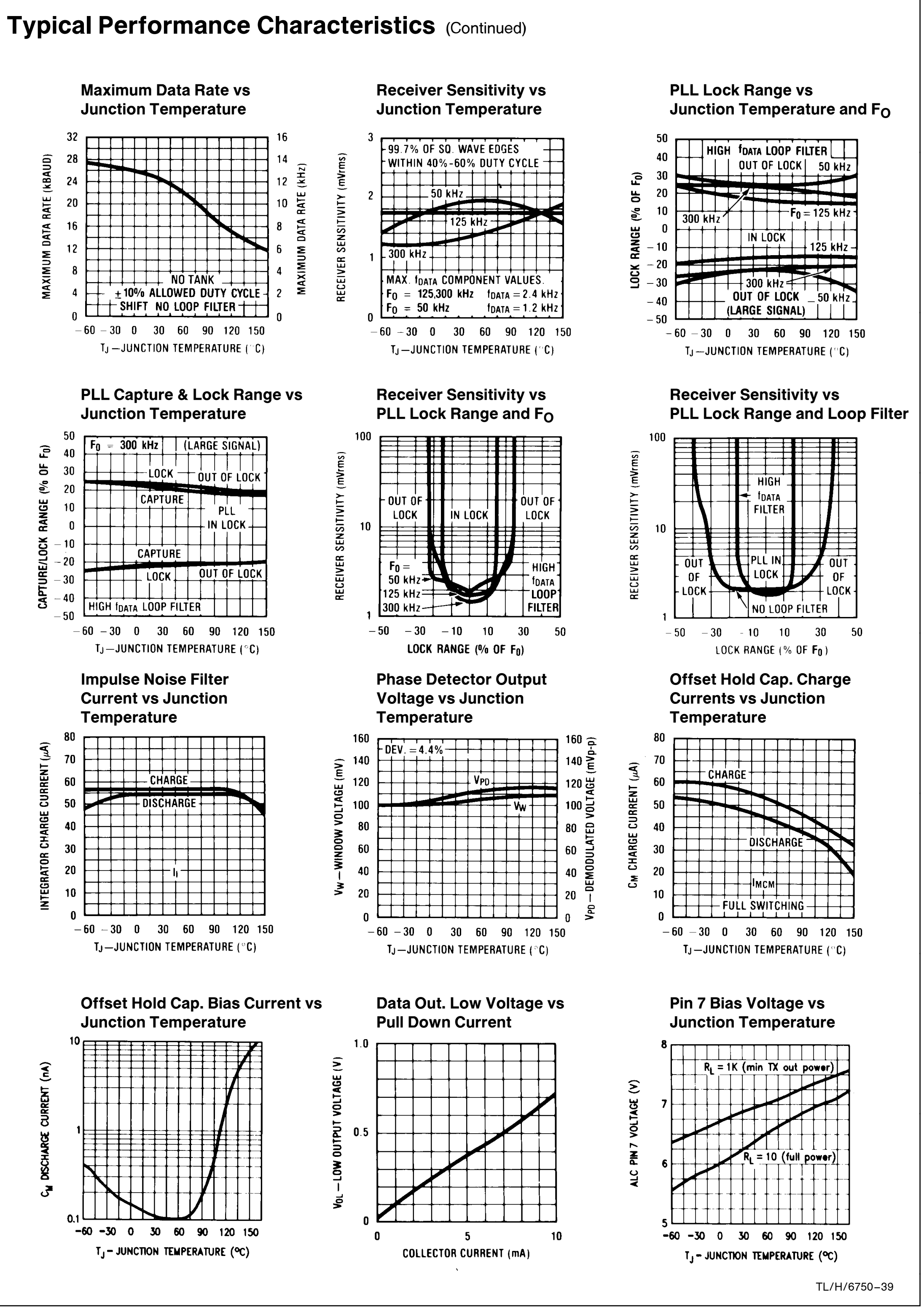
ALC Voltage vs Junction Temperature

ICO Frequency vs Junction Temperature

Transmitter FSK Deviation vs Junction Temperature

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Typical Performance Characteristics (Continued)



Application Information*

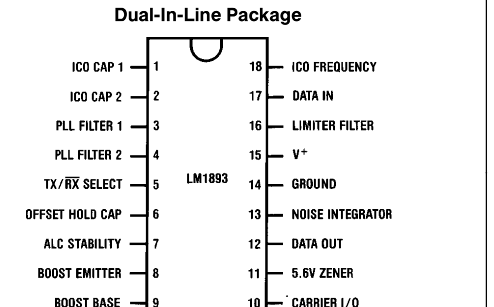
THE DATA PATH

The BI-LINE™ chip serves as a power line interface in the carrier-current transceiver (CCT) system of *Figure 3*. *Figure 4* shows the interface circuit now discussed. The controller may select either the transmit (TX) or receive (RX) mode. Serial data from the controller is used to generate a FSK-modulated 50 to 300 kHz carrier on the line in the TX mode. In the RX mode line signal passes through the coupling transformer into the PLL-based receiver. The recreated serial bit stream drives the controller.

With the IC in the TX mode (pin 5 a logic high), baseband data to 5 kHz drive the modulator's Data In pin to generate a switched 0.978I/1.022I control current to drive the low TC, triangle-wave, current-controlled oscillator to ±2.2% deviation. The tri-wave passes through a differential attenuator and sine shaper which deliver a current sinusoid through an automatic level control (ALC) circuit to the gain of 200 current output amplifier. Drive current from the Carrier I/O develops a voltage swing on T_1's (*Figure 4*) resonant tank proportional to line impedance, then passes through the step-down transformer and coupling capacitor C_C onto the line. Progressively smaller line impedances cause reduced signal swing, but never clipping-thus avoiding potential radio frequency interference. When large line impedances threaten to allow excessive output swing on pin 10, the ALC shunts current away from the output amplifier, holding the voltage swing constant and within the amp's compliance limit. The amplifier is stable with a load of any magnitude or phase angle.

In the RX mode (pin 5 a logic low), the TX sections on the chip are disabled. Carrier signal, broad-band noise, transient spikes, and power line component impinge of the receiver's input highpass filter, made up of C_C and T_1, and the tank bandpass filter. In-band carrier signal, band-limited noise, heavily attenuated line frequency component, and attenuated transient energy pass through to produce voltage swing on the tank, swinging about the positive supply to drive the Carrier I/O receiver input. The balanced Norton-input limiter amplifier removes DC offsets, attenuates line frequency, performs as a bandpass filter, and limits the signal to drive the PLL phase detector differentially. The differential demodulated output signal from the phase detector, containing AC and DC data signal, noise, system DC offsets, and a large twice-the-carrier-frequency component, passes through a 3-stage RC lowpass filter to drive the offset cancel circuit differentially. The offset cancelling circuit works by insuring that the (fixed) ±50 mV signal delivered to the data squaring ("slicing") comparator is centered around the 0 mV comparator switch point. Whenever the comparator signal plus DC offset and noise moves outside the carefully matched ±50 mV voltage "window" of the offset cancel circuit, it adjusts its DC correction voltage in series with the differential signal to force the signal back into the window. While the signal is within the ±50 mV window, the DC offset is stored on capacitor C_M. By grace of the highly non-linear offset hold capacitor charging during offset cancelling, the DC cancellation is done much more quickly than with an AC coupling capacitor normally used in place of the offset cancel circuit. Since impulse noise spikes normally ring the signal symmetrically around 0 V, the fully bilateral offset cancel topology affords excellent noise rejection. The switched current output of the comparator drives the impulse noise filter integrator capacitor that rejects all data pulses of less than the integrator charge time. Noise appears as duty-cycle jitter at the open collector serial data output.

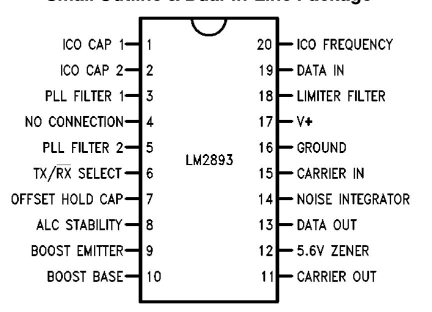
Dual-In-Line Package



Top View

Order Number LM1893N
See NS Package Number N18A

Small Outline & Dual-In-Line Package



Top View

Order Number LM2893M or LM2893N
See NS Package Number M20B or N20A

FIGURE 2. Connection Diagrams

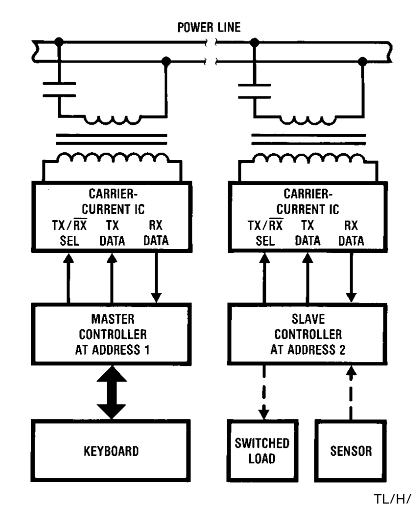


FIGURE 3. The block diagram of a carrier-current system using the Bi-Line chip to interface digital controllers via the power line

*Unless otherwise noted, all pin references refer to LM1893, but hold true for equivalent LM2893 pin.

Application Information (Continued)

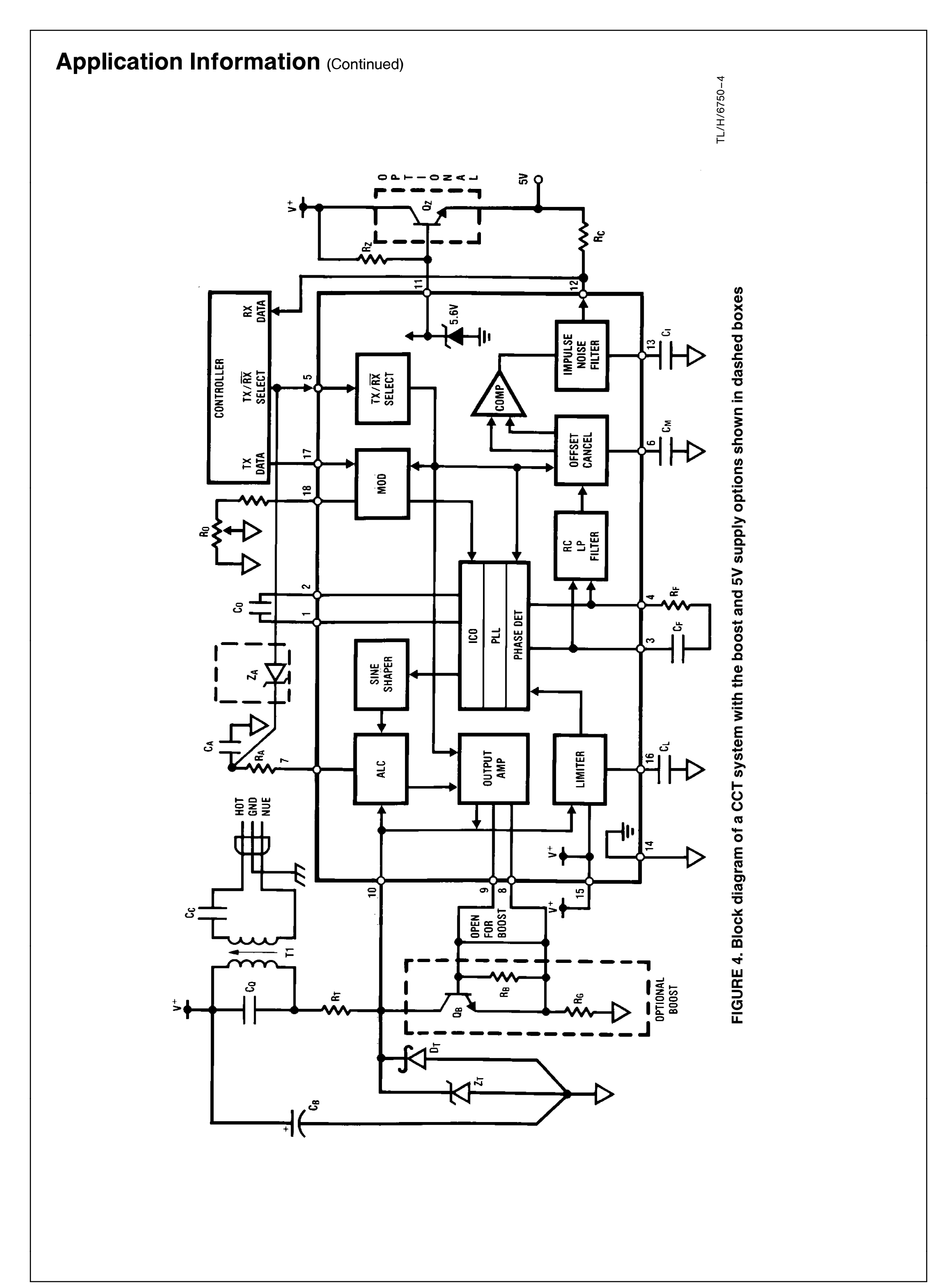


FIGURE 4. Block diagram of a CCT system with the boost and 5V supply options shown in dashed boxes

Application Information (Continued)

#	Recommended Value	Purpose	Effect of making the component value:		Notes
			Smaller	Larger	
C_O R_O	560 pF 6.2 kΩ	Together, C_O and R_O set ICO F_O.	Increases F_O Increases F_O <5.6 k not recommended.	Decreases F_O Decreases F_O >7.6 k not recommended.	±5% NPO ceramic. Use low TC 2 k pot and 5.6 k fixed R. Poor F_O TC with <5.6 k R_O.
C_F R_F	0.047 µF 3.3 kΩ	PLL loop filter pole PLL loop filter zero	Less noise immune, higher f_{DATA}, more PLL stability. PLL less stable, allows less C_F. Less ringing.	More noise immune, lower f_{DATA}, less PLL stability. PLL more stable, allows more C_F. More ringing.	Depending on R_F value and F_O, PLL unstable with large C_F. See Apps. Info. C_F and R_F values not critical.
C_C	0.22 µF	Couples F_O to line, C_C and T_1 low-pass attenuates 60 Hz.	Low TX line amplitude. Less 60 Hz T_1 current. Less stored charge.	Drives lower line Z. More 60 Hz T_1 current. More stored charge.	≥250 V non-polar. Use $2C_C$ on hot and neutral for max. line isolation, safety.
C_Q T_1	0.033 µF Use recommended XFMR	Tank matches line Z, bandpass filters, isolates from line, and attenuates transients.	Tank F_O up or increase L of T_1 for constant F_O. Smaller L: higher F_O or increase C_C; decreased F_O line pull.	Tank F_O down or decrease L of T_1 for constant F_O. Larger L: lower F_O or decrease C_C; increased F_O line pull.	100 V nonpolar, low TC, ±10% High large-signal Q needed. Optimize for low F_O line pull with control of F_O TC and Q.
C_A R_A	0.1 µF 10 kΩ	ALC pole ALC zero	Noise spikes turn ALC off. Less stable ALC.	Slower ALC response. More stable ALC.	R_A optional. ALC stable for $C_A \geq 100$ pF.
C_L	0.047 µF	Limiter 50 kHz pole, 60 Hz rejection.	Higher pole F, more 60 Hz reject. F_O attenuation?	Lower pole F, less 60 Hz reject, more noise BW.	Any reasonably low TC cap. 300 pF guarantees stability.
C_M	0.47 µF	Holds RX path V_{OS}	Less noise immune, shorter V_{OS} hold, faster V_{OS} aquisition, shorter preamble.	More noise immune, longer V_{OS} hold, slower V_{OS} aquisition, longer preamble.	Low leakage ±20% cap. Scale with f_{DATA}.
C_I	0.047 µF	Rejects short pulses like impulse noise.	Less impulse reject, less delay, more pulse jitter.	More impulse reject, more delay, less pulse jitter.	C_I charge time ½ bit nom. Must be <1 bit worst-case.
R_C	10 kΩ	Open-col. pull-up	Less available sink I.	Less available source I.	$R_C \geq 1.5$ kΩ on 5.6 V
R_Z	12 kΩ	5.6 V Zener bias	Larger shunt current, more chip dissipation.	Smaller shunt current, less V^+ current draw.	$1 < I_Z < 30$ mA recommended. (Chip power-up needs 5.6 V)
Z_T R_T D_T	≥44 V BV <60 V peak 4.7 Ω ≥44V BV	Transient clamp Transient I limit Over-drive Clamp	Z_T failure, higher series R-excess peak V, Zener and chip damage, less ruggedness. Damage Z_T, pull up V^+. Failure on Transient	Z_T costly, lower series R gives enhanced transient clamp, more ruggedness. Excessive TX attenuation. Costly	Recommend Zener rated for ≥500 W for 1 ms. Carbon comp. recommended. IRF 11DQ05 or 1N5819
R_B Q_B R_G	180 Ω Power NPN 1.1 Ω	Base bleed Boost gain device Current setting R	Faster, lower THD I_O. Excessive T_J and V_{SAT}. More I_O, need higher h_{fe}.	Inadequate turn-off speed. More rugged, but costly. Less I_O, lower min. h_{fe}.	Boost optional. Q_B F(−3 dB) of >200 MHz. R_B > 24 Ohm. $I_O = 70[(10 + R_G)/R_G]$ mApp.
C_B	≥47 µF	Supply bypass	Transients destroy chip.	Less supply spike.	V^+ never over abs. max.
Z_A	5.1V	Stop ALC charge in RX mode	Excess ALC current flow	ALC RX charging not inhibited over T_J	Z_A optional - 5.1V ±20% low leakage type

FIGURE 5. A quick explanation of the external component function using the circuit of *Figure 4*. Values given are for $V^+ =$ 18 V, $F_O = 125$ kHz, $f_{DATA} = 360$ Baud (180 Hz), using a 115 V 60 Hz power line

Component Selection

Assuming the circuit of *Figure 4* is used with something other than the nominal 125 kHz carrier frequency, 180 Hz data rate, 18V supply voltage, etcetera, the component values listed in *Figure 5* will need changing. This section will help direct the CCT designer in finding the required component values with emphasis placed on look-up tables and charts. It is assumed that the designer has selected values for carrier center frequency, F_O; data rate, f_{DATA}; supply voltage, V^+; power line voltage, V_L; and power line frequency, F_L. If one or more of those parameters is not defined, one may read the data sheet and make an educated guess.

Maxims to keep in mind, based on CCT electrical performance considerations only, are: 1) the higher the F_O the better, 2) the lower the maximum data rate the better, and 3) the more time and frequency filtering the better.

Use *Figure 5* as a quick reference to the external component function.

THE TRANSMITTER

C_O

Central to chip operation is the low TC of F_O emitter-coupled oscillator. With proper C_O, the F_O of the $2V_{BE}$ amplitude triangle-wave oscillator output may vary from near DC to above 300 kHz. While C_O may have any value, C_O should

Component Selection (Continued)

be made above 10 pF so that parasitic capacitance is not dominant. Excessive or unbalanced common-mode-to-ground capacitance should be avoided. A low temperature coefficient (TC) of capacitance (<100 PPM/°C), such as a monolithic NPO ceramic multilayer type, preserves low TC of F_O. *Figure 6* finds a C_O value given F_O.

R_O

Resistor R_O is used by the IC to generate a V_{BE}/R related current that is multiplied by 2 to produce the 200 μA ICO control current that sets F_O. The control current TC "bucks" the V_{BE} related tri-wave amplitude across C_O to effect a low TC of F_O. Vary R_O to trim F_O, within limits. Raising F_O more than 20% above its untrimmed value by means of decreasing R_O more than 20% is not recommended. Low R_O, and so high control current, risks ICO saturation and poor TC under worst-case conditions. Raising R_O reduces the demodulated signal amplitude from the phase detector; raising R_O by more than a factor of 2 (1 octave) is not recommended.

Since lower TC pots are relatively costly, it is recommended that R_O be made up of a 5.6 k fixed (<100 PPM/°C) resistor with a 2 kΩ (<250 PPM/°C) series pot.

C_A and R_A

Components C_A and R_A control the dynamic characteristics of the transmitter output envelope. Their values are not critical. Use the values given in *Figure 5*. C_A and R_A are functions of loaded T_1 tank Q, R_O, f_{DATA}, and line impulse noise. Any changes made in C_A and R_A should be made based on empirical measurements of a CCT on the line. Roughly, C_A acts as an ALC pole and R_A an ALC zero.

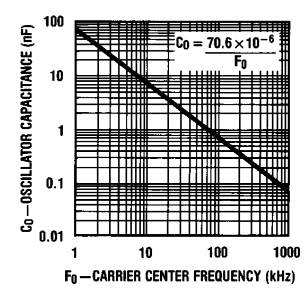
T_1

At this point, the CCT system designer may choose to use one of the recommended transformers or to design custom T_1. Consult "The Coupling Transformer" section to help with the design of T_1 if a new or boost-capable transformer is needed. The recommended 125 kHz transformer functions with an I_O of up to 600 mApp.

It is recommended that CCT systems use the recommended transformers, described in *Figure 7*, for T_1. The 3 transformers are optimized for use in the ranges of 50–100 kHz, 100–200 kHz, and 200–400 kHz with unloaded Q's (Q_U) of about 35, and loaded Q's (Q_L) of about 12. Three secondary taps are supplied with nominal 7.07, 10, and 14.1 turns ratios (N) to drive industrial and residential power line impedances of 3.5, 7, and 14Ω respectively. All are inexpensive, all have the same pin-outs for easy exchange in a PC board, and all are small - on the order of 10 mm diameter at the base.

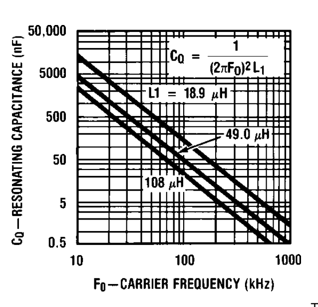
C_Q

Tank resonant frequency F_Q must be correct to allow passage of transmitter signal to the line. Use *Figure 8* to find C_Q's value. Trimming F_Q to equal F_O is done with T_1's trimming slug. The inductance of T_1 has a TC of +150 PPM/°C which may be cancelled by using a −150 PPM/°C cap such as polystyrene. Since circulating current in the tank is ¼ A_{RMS}, C_Q should have a low series resistance (a 1 Ω series resistance is too much). Polypropelene caps are excellent, "orange drop" mylars are adequate, while many other mylars are inadequate. A 100V rating is needed for transient protection.



TL/H/6750–5

FIGURE 6. Find C_O's value knowing F_O



TL/H/6750–10

FIGURE 8. Find C_Q's value given F_O

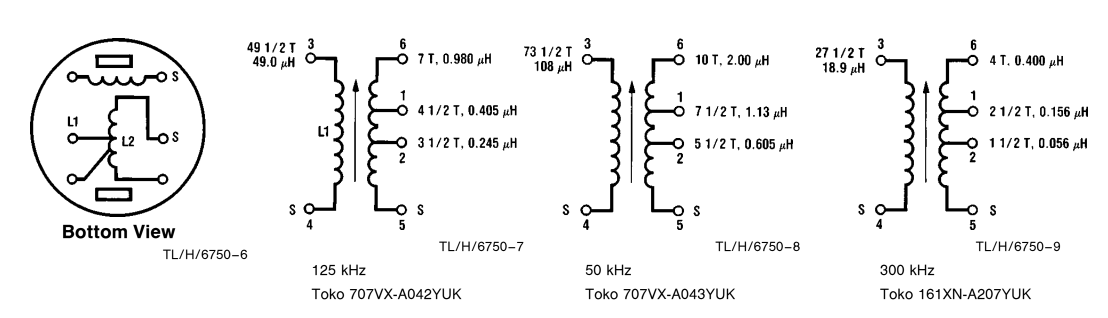


FIGURE 7. The recommended T_1 transformers, available through:
Toko America, 1250 Feehanville Drive, Mount Prospect, IL, 60056, (312) 297-0070

Component Selection (Continued)

C_C

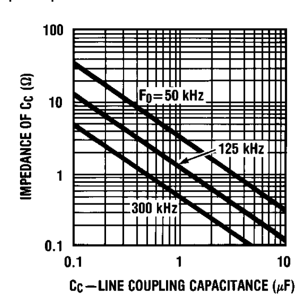
Capacitor C_C's primary function is to block the power line voltage from T_1's line-side winding. Also, C_C and T_1's line-side winding comprise a LC highpass filter. The self-inductance of T_1 is far too low to support a direct line connection. C_C must have a low enough impedance at F_O to allow T_1 to drive transmitted energy onto the line. To drive a 14Ω power line, the impedance of C_C should be below 14Ω.

Use *Figure 9* to find the reactive impedance of C_C to check that it is less than the line impedance. Then check *Figure 10* to see that the power line current is small enough to keep T_1 well out of saturation; the recommended transformers can withstand a 10 Amp-turn magnetizing force (1 Amp through the worst-case 10 turn line-side winding).

Caution is required when choosing C_C to avoid series resonance of the series combination of C_C, the transformer inductance, and the reflected tank impedance. The low resistance of the network under series resonance will load the line, possibly decreasing range. For your particular line coupling circuit, measure for series resonance using some expected line impedance load.

R_B

This base-bleed resistor turns Q_B off quickly - important since the amplifier output swing is about 200V/µs. An R_B below about 24Ω will conduct excessive current and overload the chip amplifier and is not recommended.



TL/H/6750–11

FIGURE 9. C_C's impedance should be, as a rule-of-thumb, smaller than the lowest expected line impedance

R_G

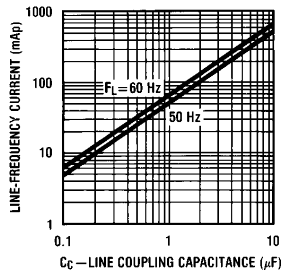
This resistor, in parallel with the internal 10Ω resistor, fixes the current gain of the output amplifier, and so the output current amplitude. *Figure 11* gives output current and minimum AC current gain h_{fe} for Q_B when R_G is used to boost output current.

Q_B

The boost gain transistor Q_B must be fast. Double-diffused devices with 50 MHz F_T's work, slower transistors (epi-base types) do not preserve a sinusoidal waveform when F_O is high or will cause the output amp. to oscillate. Q_B must have a certain minimum h_{fe} for given boost levels, as shown in *Figure 11*. *Figure 12* shows the power Q_B must dissipate continuously operating with a shorted output. BV_{CER} ($R = R_B$) must be 60V or greater and Q_B must have adequate SOA for transient survival.

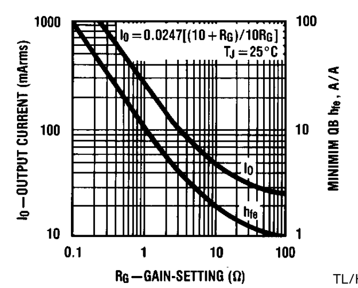
Z_T

Unfortunately, potentially damaging transient energy passes through transformer T_1 onto the Carrier I/O pin (instantaneous power of greater than 1 kW has been measured using the recommended transformers). For self protection, the Carrier I/O has an internal 44V voltage clamp with a 20Ω series resistance. A parallel low impedance 44V external transient suppression diode will then conduct the lion's share of any current when transients force the Carrier I/O to a high voltage.



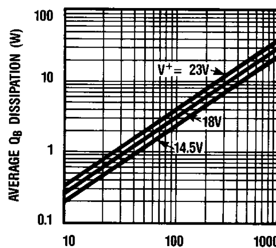
TL/H/6750–12

FIGURE 10. The AC line-induced current passed by C_C



TL/H/6750–13

FIGURE 11. Output amplifier current and required min. Q_B h_{fe} versus gain-setting resistor R_G



TL/H/6750–14

FIGURE 12. Boost transistor power dissipation versus amplifier output current

Z_T must be used unless some precaution is taken to protect the Carrier I/O pin from line transients or transients caused when stored line energy in C_C is discharged by the random phase of power line connection and disconnection. Worst case, C_C may discharge a full peak-to-peak line voltage into the tuned circuit. Another way to reduce the need for Z_T is by placing another magnetic circuit in the signal path that relies on a high, but easily saturated, permeability to couple a primary and secondary winding - a toroidal transformer for example. Toroids cost more than Z_T.

Use an avalanche diode designed specifically for transient suppression — they have orders of magnitude higher pulse

Component Selection (Continued)

power capability than standard avalanche diodes rated for equal DC dissipation. Metal oxide varistors have not proven useful because of their inferior clamping coefficient and are not recommended. Specifications for an example minimum diode are given in *Figure 13*.

Breakdown Voltage	44–49V @ 1 mA
Maximum Leakage	1 μA @ 40V
Capacitance	300 pF @ BV
Maximum Clamp Voltage	64.5V @ 7.8A
Peak Non-Repetitive Pulse Power	10 kW for 1 μs
(REA Standard Exponential Pulse)	
Surge Current	70A for 1/120s

FIGURE 13. Key specifications for a recommended transient suppressor Z_T available from General Semiconductor, 2001 West Tenth Place, Tempe, AZ 85281, 602–968-3101, part no. SA40A

R_T

R_T acts as a voltage divider with Z_T, absorbing transient energy that attempts to pull the Carrier Input pin above 44V. Make the resistor a carbon composition 1/4W. When experiments discharging C_C charged to the peak-to-peak 620V AC thru a 1Ω power line were carried out, film resistors blew open-circuit.

D_T

This Schottky diode is placed in parallel with the CCT chip's substrate diode to pass the majority of the current drawn from ground when the Carrier Input or Carrier Output is pulled below ground by a larger-than-twice-the supply-swing on the tank. Note that Z_T is in parallel with the substrate diode, but is ineffective due to its high forward voltage drop and high diffusion capacitance caused by its low forward speed. Tests proved that a 1N5818 kept a receive-path functional with a 20X boost transmitter with a 7:1 transformer attempted to swing the receiver's Carrier I/O to ±100V (300 mA peak ground current in the receiver). Without D_T, the receiver momentarily stops functioning at a 100 times lower ground current.

This diode is not needed if the Carrier I/O never swings below ground. If your CCT systems all run on the same regulated voltage with all matched transformers and turns ratios, it is not needed. Otherwise, it is.

THE RECEIVER

The receiver and transmitter share components C_C, T_1, C_Q, R_T, Z_T, C_O, R_O, and peripheral supply and bias components that are not in need of change for RX mode operation. Values for the balance of the components are now found.

Line-Frequency Rejection

To use the ultimate sensitivity of the device, fully 110 dB of 115 V, 60 Hz attenuation is required between the line and the limiter amplifier output. Using the circuit topology of *Figure 4*, the combined attenuation of the C_C/T_1 highpass, the tuned transformer, and the bandpass filter attenuation of the limiter amplifier give far more line rejection than the above-stated minimum. However, if some other CCT line coupling circuit is used, line rejection will become important to the system designer.

Receiver input power supply rejection (PSRR) and common-mode rejection (CMRR) are one-in-the-same using the supply-referenced signal input of *Figure 4*. Ripple swings both differential inputs of the Norton amp. equally, while the single-ended input signal swings only the positive input. Overall PSRR consists of the input CMRR (set by the input stage component matching) and the ripple-frequency attenuation of the input amplifier bandpass response that passes carrier frequency but stops low frequencies. A typical 1% resistor and 1 mV n-p-n mirror offsets give 26 dB of attenuation, the bandpass gives 54 dB 120 Hz attenuation, for an overall 80 dB PSRR to allow tens of volts of ripple before impacting ultimate sensitivity.

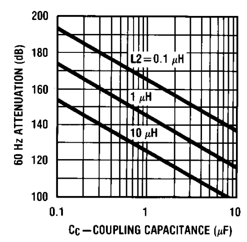
C_C

A value was chosen earlier. Knowing T_1's secondary inductance allows a check of LC line attenuation using *Figure 14*.

C_L

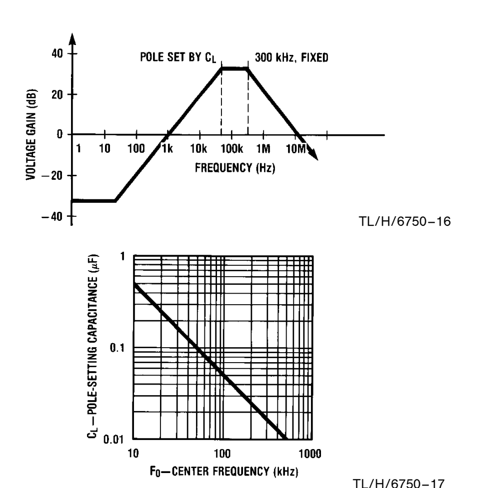
The Norton input limiter amplifier has a bandpass filter for enhanced receiver selectivity, noise immunity, and line frequency rejection. The nominal response curve for $F_O = 50$ kHz is shown in *Figure 15*. The 300 kHz pole is fixed. The 50 kHz pole is set by C_L's value. After C_L is found, the resulting line frequency attenuation is found for the bandpass filter.

Use *Figure 15* to find a C_L value given for F_O. The approximate line frequency attenuation of the bandpass filter may then be found in *Figure 16*. *Figure 15* returns a value for C_L 33% larger than nominal, giving a low frequency pole 33% low to allow for component tolerances.



TL/H/6750–15

FIGURE 14. The 60 Hz line rejection of the highpass filter made up of C_C and T_1's line-side winding (neglecting capacitive coupling)



TL/H/6750–16

TL/H/6750–17

FIGURE 15. Given F_O, C_L is found. Also shown is the input amplifier's small signal amplitude response

C_F and R_F

These phase-locked loop (PLL) loop filter components remove some of the noise and most of the $2F_O$ components present in the demodulated differential output voltage signal from the phase detector. They affect the PLL capture range, loop bandwidth, damping, and capture time. Because the PLL has an inherent loop pole due to the integrator action of the ICO (via C_O), the loop pole set by C_F and the zero set by R_F gives the loop filter a classical 2nd-order response.

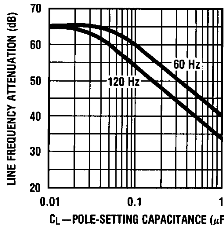


FIGURE 16. The Norton-input limiter amplifier bandpass filter line-frequency signal attenuation given C_L

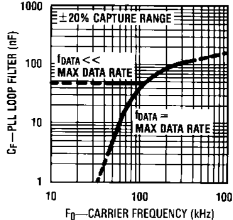


FIGURE 17. Find C_F given F_O. *Figure 19* gives the maximum data rate

No C_F and R_F give the most stable PLL with the fastest response. Large C_F's with a too-small R_F cause PLL loop instability leading to poor capture range and poor step response or oscillation.

Calculation of C_F and R_F is quite difficult, involving not only the 2nd-order loop step response, but also the PLL non-dominant poles, the tuned transformer stepped-frequency response, and the RC lowpass step response (for data rates approaching 1 kHz). C_F and R_F values are best found empirically. Tolerance is not critical. Component values are selected to give the best possible impulse noise rejection while preserving a ±20% capture range and wide stability margin. *Figures 17* and *18* give C_F and R_F values versus F_O, where "f_{DATA} << MAX DATA RATE" means that f_{DATA} should be less than the maximum data rate, in kHz, from *Figure 19* divided by 10.

Note that C_F and R_F are a function of data rate only for high data rates and are not plotted against data rate - as one might expect. The reason for this is important to understand if the CCT system designer wishes to find C_F and R_F empirically. Data signal is, loosely speaking, passed through the PLL loop and is therefore potentially attenuated if the loop bandwidth is on the order of the 3rd harmonic of the data rate, or less. Overall loop bandwidth is held as low as possible for maximum noise rejection while passing the data. Loop bandwidth is roughly proportional to the geometric mean of the unfiltered loop bandwidth and the filter pole set by C_F. Therefore, C_F is related to data rate. Unfortunately, the loop capture range falls to critically low values when large enough values of C_F are used to reduce loop bandwidth down to the 100's of Hz range, for low data rates. The obvious way out is to then reduce the unfiltered loop bandwidth. That bandwidth is approximately proportional to the value of C_O. For a fixed F_O, unfiltered loop bandwidth reduction requires a larger C_O and larger control current. With this chip, changing the control current is not allowed. So one is forced to choose a C_F/R_F combination with some minimum capture range, say ±20%, that is within some guardband from the point of loop instability. Happily, impulse noise tends to last only fractions of a millisecond so that the lack of low bandwidth loop response with low data rates is not a heavy penalty. As long as there is adequate capture range, the impulse noise filter performs admirably. Note that reducing F_O will reduce the no-filter loop bandwidth, and indeed the maximum data rate falls below the limit set by the RC lowpass filter as F_O falls below 100 kHz (*Figure 19*).

The tuned transformer characteristics will affect the demodulated data waveform more than C_F and R_F at low data rates. Tank Q and off-tuning will affect overshoot during the FSK frequency steps. This is a property of tuned circuits. The maximum data rate of *Figure 19* is measured from the receiver input to the Data Out and does not include the data bandwidth reducing effects of T_I.

C_M

Capacitor C_M stores a voltage corresponding to a correction factor required to cancel the phase detector differential output DC offsets. The stored voltage is 5⁄6 of the DC offset plus some bias level of about 2.2 V. A large C_M value increases the time required to bias-up the receive path at the beginning of transmission. A large C_M does filter well and store its bias voltage long. Because of the initial random charge of C_M, the receiver must be given a data transition to charge to the proper bias voltage. Therefore, reducing C_M's value to one that may be charged in less than 2 bit-times will not save biasing time and is not recommended.

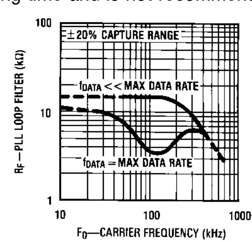


FIGURE 18. Find R_F given F_O with F_{DATA} a parameter

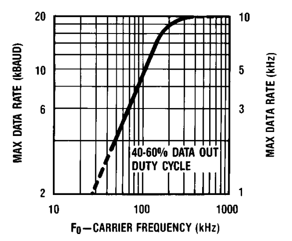
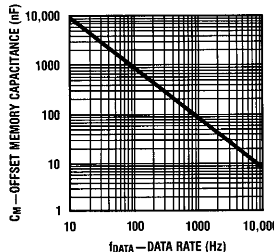


FIGURE 19. The maximum data rate versus F_O using loop filter components optimized for max. noise performance while retaining a min. ±20% capture range (large signal)

Use *Figure 20* to find C_M's value knowing f_{DATA}, assuming the standard 2 bit receive charge time is desired. The cap. value and TC are not critical, but the capacitor should have low leakage.

Component Selection (Continued)



TL/H/6750–22

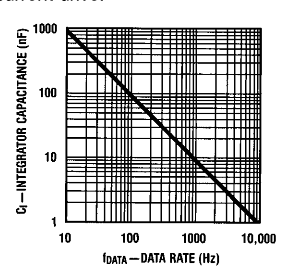
FIGURE 20. Size C_M assuming a 2 bit-time receive bias time

C_I

The impulse noise filter integrator capacitor C_I is used to disallow the passage of any pulse shorter than the integrator charge time. That charge time, set to a nominal ½ bit time, is the time required for a $\pm 50\ \mu A$ charge current to swing C_I over a 2 V_{BE} range. Charge time under worst case conditions must never be greater than a bit time since no signal could then pass. Using a $\pm 10\%$ capacitor, full junction temperature range, and full specified current range, a maximum nominal charge time of ½ bit is recommended. *Figure 21* gives C_I versus data rate under those conditions.

R_C

The collector pull-up resistor is sized to supply adequate pull-up current drive and speed while preserving adequate output low current drive.



TL/H/6750–24

FIGURE 21. Impulse noise filter cap. C_I versus F_{DATA} where the charge time is ½ bit time

Z_A

The 5.1V silicon zener diode Z_A is required when a short RX-to-TX switch-over time is needed at the same time that the chip is operating in the RX mode with a pin 10 input signal swing approaching or exceeding twice the supply voltage. Predominant causes of these large swings impinging on the RX input are: 1) a transmitter's supply voltage higher than the receiver's supply voltage, 2) a TX and RX pair that are electrically close, or, 3) a higher RX T_1 step-up turns ratio than the TX T_1 step-down ratio.

Normally, when in the RX mode with small incoming signal on pin 10, the ALC remains off with pin 7 at a 6V ($V_Z - 2V_{BE}$) bias voltage. C_A is then charged to 6V. TX mode may then be selected with 6V on C_A allowing 100% TX power to pump T_1's tuned circuit, and so the AC line, quickly for fast RX-to-TX switch time. As TX output swing increases so that pin 10 swings below V_{ALC} (4.7V typically), that ALC activates to charge C_A to about 6.6V to reduce TX output drive. However, if in the RX mode pin 10 ever swings below V_{ALC}, C_A will charge to above 6.6V. Now, when the TX mode is selected with C_A at 6.6V, somewhere from 0 to 100% TX output drive is available to pump T_1's tuned circuit resulting in a slower rising line signal - effectively reducing the RX-to-TX switch time.

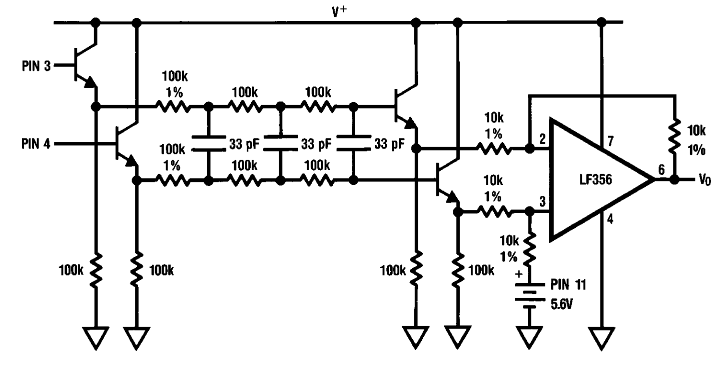
Use a 5.1V Z_A driven by a 0 to 0.8V logic low signal to guarantee over-temp. operation. R_A must be in series with Z_A to limit current flow and should never fall below 1 kΩ. If R_A is less than 1 kΩ, then put a 2 kΩ resistor in series with Z_A. Logic high voltages above 10V will cause current flow into pin 7 that must be limited to 1 mA (with R_A or a series R).

Breadboarding Tips

During CCT system evaluation, some techniques listed below will simplify certain measurements.

— Use caution when working on this circuit - dangerous line voltages may be present.

— When evaluating PLL operation, offset cancel circuit operation, and loop filter values, use the filter of *Figure 22* to view the demodulated signal minus the $2F_O$ and noise components. This filter models the RC lowpass filter on chip.



TL/H/6750–25

FIGURE 22. Circuit to view the differential demodulated data signal, minus the noise and $2F_O$ components, conveniently with a single-ended gain-of-one output

Breadboarding Tips (Continued)

— When evaluating CCT system noise performance on a real power line, it is desirable to vary the signal amplitude to the receiver. This is not easy. An in-line line-proof L-pad is fine except that the line impedance is unknown and variable and so the L-pad will rarely match. Instead, the power output of a chip transmitter may be controlled using the circuit of *Figure 23*. This circuit controls the ALC.

— It is sometimes desirable to place impulse noise on the line. A simple light dimmer with a 100 W light bulb load produces representative impulse noise.

— Do not allow peak currents of over 1 A through the 5.6 V Zener. In other words, don't short charged capacitors into this low-impedance device. Take care not to momentarily short pins 10 and 11 - chip damage may result.

— *Figure 24* shows some typical signals beginning with serial data transmitted to received signal.

Tuning Procedure

This procedure applies to circuits similar to *Figure 4* LM1893 or LM2893 circuit.

First, trim F_O by putting the chip in the TX mode, setting a logical high data input, and measuring the TX high frequency, 1.022 F_O, on the Carrier I/O using these steps:

1. Take pin 17 to a logic low.
2. Take pin 5 to a logic high.
3. Place a counter on pin 10.
4. Adjust R_O on pin 18 for $F = 1.022F_O$.

Second, the line transformer is tuned. The chip is placed in the TX mode, a resistive line load is connected to disable the ALC by reducing tank voltage swing below its limit. FSK data is then passed through the tank so that the tank envelope may be adjusted for equal amplitude for high and low data frequency.

1. Take pin 5 to a logic high.
2. Place a logic-level square wave at or below the receiver's maximum data rate on pin 17.
3. Temporarily place a 330 Ω resistor across the tank.
4. Place a scope on pin 10.
5. Adjust the transformer slug for the least envelope modulation.

In lieu of the 330 Ω resistive load, T_1 may be coupled to the power line to better simulate actual load and tank pull conditions during tank tuning. Alternatively, a passive network representing an average line impedance may be connected to the line side of T_1. The circuit of *Figure 23* should then be used to defeat the leveling effect of the ALC.

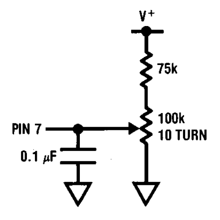


FIGURE 23. A means of transmitter output amplitude control is shown

Thermal Considerations

It is desirable to place the largest possible signal on the power line for maximum range, limited only by the chip power dissipation and maximum junction temperature T_J. The falling output power at elevated T_J allows a more optimal power output - high power at low T_J and lower power at high T_J for chip self-protection. However, it is still possible to exceed the maximum T_J within the specified ambient temperature limit ($T_A = 85°C$) under worst case conditions of 100% TX duty cyle, high supply, shorted load, poor PC board layout (with small copper foil area), and an above nominal current part. Under those conditions, a part may dissipate 2140 mW, reaching a $T_J = 170°C$ worst-case (admittedly a rare occurrence). Proper system design includes the measurement or calculation of T_J max. to guarantee function under worst-case operation. Like all devices with failure modes modeled by the Arrhenius model, the high chip reliability is further enhanced by keeping the die temperature mercifully below the absolute maximum rating.

A direct method of measuring operating junction temperature is to measure the V_{BE} voltage on pin 18, which is always available under all operating modes. The graph of *Figure 25* may be used to find T_J, knowing V_{BE} at the operating point in question and V_{BE} at $T_A = T_J = 25°C$. V_{BE} is found by powering up a chip (in RX mode) that has been dissipating zero power at some T_A for some time and measuring V_{BE} in less than 1 s (for better than 5°C accuracy).

Alternately, T_J may be calculated using:

$$T_J = T_A + \theta_{JA} P_D \quad (1)$$

where θ_{JA} is 75°C/W for the plastic (N) package using a socket. That θ_{JA} value is for a high confidence level; nomi-

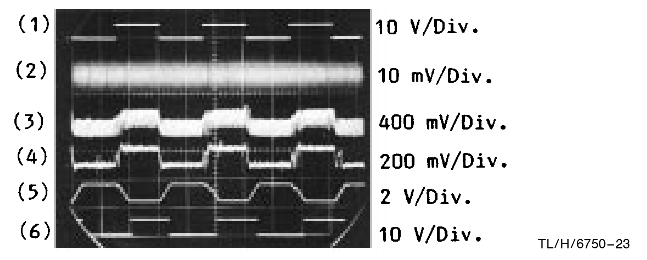


FIGURE 24. Oscillogram revealing signals at several important nodes under weak signal (0.5 mV_{RMS}) conditions with SCR spikes on an otherwise quiet 115 V, 60 Hz power line. The signals are: 1) transmitted data, 2) RX carrier on the tuned transformer, 3) demodulated signal from the PLL after passing thru circuit of *Figure 22*, 4) signal after RC lowpass, 5) data at impulse noise filter integrator, and 6) received data. Horizontal scale is 10 ms per div.

Thermal Considerations (Continued)

nal θ_{JA} for an N package is 60°C/W, lower with good PC board layout. Since P_D is a relatively strong function of T_J, an iterative solution process starting with an initial guess for T_J is used. With the estimated T_J, find the total supply current found in the typical performance characteristics.

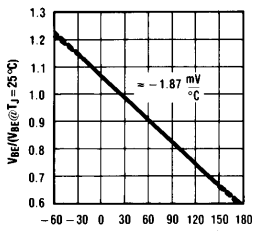


FIGURE 25. T_J may be found by using the temperature coefficient of pin 18 V_{BE} if V_{BE} is known at 25°C

Transmit-To-Receive Switch-Over Time

An important figure-of-merit for a half-duplex CCT link, affecting effective data rate, is the TX-to-RX switch time T_{TR}. Using the recommended component values gives this part a nominal 2 bit-time (1 bit time = $1/[2f_{DATA}]$) over a wide range of operating conditions, where the receiver requires 1 data transition. T_{TR} cannot be decreased significantly but does increase as noise filtering, especially via C_M, is increased. Impulse noise at switch, signals near the limiting sensitivity, poor F_O match between receiver and transmitter because of poor trim or worst-case conditions, and the statistical nature of PLL signal acquisition may all contribute to increase T_{TR} to possibly 4 bit-times.

T_{TR} is lower when a pair of LM1893's handshake rapidly. The receiver was designed to "remember" the RX-mode DC operating points on C_M and C_F while in the TX mode. Under noisy worst case conditions, C_M will discharge to the point of false operation after 35 bit-times in the TX mode (1400 bit times with no noise and a nominal part, f_{DATA} = 180 Hz). T_{TR} is about 0.8 ms (proportional to the selected F_O) plus ½ bit-time.

The major components of T_{TR} are described below for a nominal 125 kHz F_O, 180 Hz f_{DATA}, lightly-loaded tank with a Q of 20, and the circuit of *Figure 4*. The remote CCT has been operating in the TX mode with a 26.6 V_{PP} tank swing and is now selected as a receiver. An incoming signal requiring the ultimate receiver sensitivity immediately is placed on the line.

First, the tank stored energy at the transmit frequency must decay to a level below the 2.8 mV_{PP} swing caused by the 0.14 mV_{RMS} incoming line signal containing the information to be received.

$$\text{decay time} = \frac{Q}{\pi F_O} \ln\left(\frac{V_1}{V_O}\right) =$$

$$\frac{20}{\pi \times 125\,000} \ln\left(\frac{26.6}{0.0028}\right) = 0.466 \text{ ms} \qquad (2)$$

That is 0.47 ms of delay (proportional to $1/F_O$ and Q).

Second, the PLL must acquire the signal; it must lock and settle. Acquisition time is statistical and may take any length of time, but average acquisition time depends on the loop filter components C_F and R_F and the difference in center frequencies, ΔF_O, of the TX/RX pair. Using the recommended C_F and R_F (47 nF and 6.2 kΩ) with a ±4.4% ΔF_O (a ± 100 mV DC offset on C_F and R_F), lock was measured to take less than 50 cycles of F_O. That is a 0.40 ms delay (proportional to $1/F_O$).

Acquisition is incomplete until the second order PLL loop settles. For the above-mentioned C_F and R_F, the loop natural frequency F_N and damping factor are found to be 2.3 kHz and 1.0 respectively. Settling to within ±25 mV of the ±100 mV DC offset change requires 2.7 periods of F_N, or 1.2 ms (a function of C_F and R_F).

Third, the RC lowpass filter introduces a 0.12 ms delay.

Fourth, C_M must charge up to ±(5⁄6)100 = 83 mV depending on the polarity of F_O. Borderline data squaring with zero noise immunity is possible with only ±(5⁄6) 50 mV of charging. C_M charge current is an asymptotic function approximated by assuming a 50 µA charge current and the full 83 mV charge voltage. C_M charge time is then 1.7 ms (proportional to $1/f_{DATA}$).

Fifth, the impulse noise filter adds a ½ bit-time delay. Total T_{TR} is 3.9 ms plus ½ bit-time for a total of 1.9 bit-times at 360 Baud.

Receive-To-Transmit Switch-Over Time

Assume the chip has been in the RX mode and the TX mode is now selected. In less than 10 µs, full output current is exponentially building tank swing. 50% of full swing is achieved in less than 10 cycles - or under 80 µs at 125 kHz. In the same 10 µs that the output amp went on, the phase detector and loop filter are disconnected and the modulator input is enabled. FSK modulation is produced in 10 µs after switching to TX mode.

Power Line Impedance

Irrespective of how wide the limits on power line impedance Z_L are placed, there are no guarantees. However, since the CCT design requires an estimate of the lowest expected line impedance Z_{LN} encountered for the most efficient transmitter-to-line coupling, line impedance should be measured and Z_L limits fixed to a given confidence level. Reasonable values for T_1 turns ratio, loaded Q, and tank resonant frequency pull F_Q may be found to enable a CCT system design that functions with the overwhelming majority of power lines.

A limited sampling of Z_L was made, during the LM1893 design, of residential and commercial 115V 60 Hz power line. Data was also drawn from the research of Nicholson and Malack (reference 1), among others, to produce *Figures 26* and *27*. All measured impedances are contained within the shaded portions of *Figure 27*. A nominal 3.5, 7.0 and 14 Ω Z_{LN} is used throughout the application information with a nominal 45° phase angle (0° is sometimes used for simplicity).

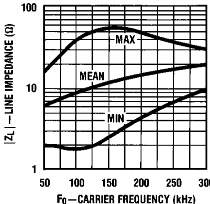
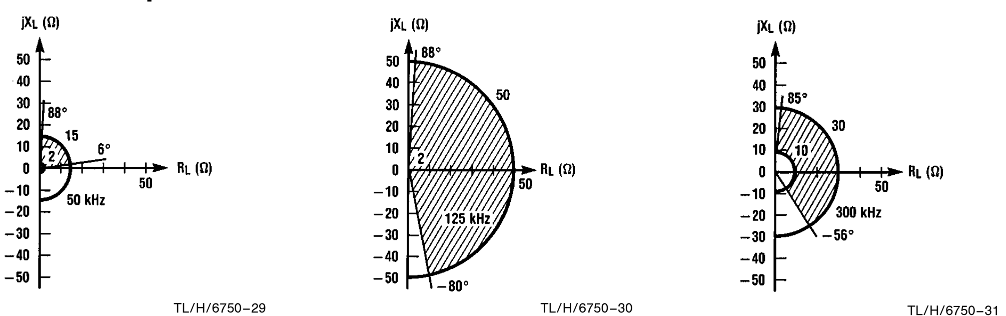


FIGURE 26. Measured line impedance range for residential and commercial 115V, 60 Hz lines

Power Line Impedance (Continued)



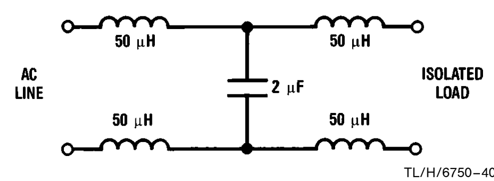
TL/H/6750–29 TL/H/6750–30 TL/H/6750–31

FIGURE 27. Complex-plane plots of measured 115V, 60 Hz line impedance where $Z_L = R_L + jX_L$

Power Line Attenuation

The wiring in most US buildings is a flat 3 conductor cable called Amerflex, BX, or Romex. All referenced line impedances refer to hot-to-neutral impedances with a grounded center conductor. The cable has a 100 Ω characteristic impedance, a 125 kHz quarter-wavelength of 600 m (250 m at 300 kHz), and a measured 7 dB attenuation for a 50 m run with a 10 Ω termination. Generally, line loads may be treated as lumped impedances. Instrument line cords exhibit about 0.7 μH and 30 pF per meter.

Limited tests of CCT link range using this chip show extensive coverage while remaining on one phase of a distribution transformer (100's of m), with link failure often occuring across transformer phases or through transformers unless coupling networks are utilized. Total line attenuation allowed from full signal to limiting sensitivity is more than 70 dB. Typically, signal is coupled across transformer phases by parasitic winding capacitance, typically giving 40 dB attenuation between phased 115 V windings. Coupling capacitors may be installed for improved link operation across phases. Power factor correcting capacitor banks on industrial lines or filter capacitors across the power lines of some electronic gear short carrier signal and should be isolated with inductors. Increasing range is sometimes accomplished by electing to install the isolating inductors (*Figure 28*) and coupling capacitors, as well as by electing to use the boost option. Frequency translating or time division multiplexed repeaters will also increase range.



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FIGURE 28. An isolation network to prevent: 1) noise from some device from polluting the AC line, and 2) to stop some low impedance device (measured at F_o) from shorting carrier signal. Component values given as an example for $F_o = 125$ kHz on residential power lines

The Coupling Transformer

The design arrived at for T_1 is the result of an unhappy compromise - but a workable one. The goals of 1) building T_1 with a stable resonant frequency, F_Q, that is little affected by the de-tuning effect of the line impedance Z_L, and of 2) building a tightly line-coupled transformer for transmitted carrier with loose coupling for transients, are somewhat mutually exclusive. The tradeoffs are exposed in the following example for the CCT designer attempting a new boost-capable, or different core, transformer design.

The compromises are eased by separating the TX output and RX input in the LM2893. An untuned TX coupling transformer with only core coupling (not air-coupled solenoid windings) would employ a high permeability, high magnetic field, low loss, square saturating, toroidal core. The resonant RX path would be isolated from line-pull problems by a unilateral amplifier that operates at line voltages with much more than 110 dB of dynamic range, or by a capacitively coupled pulse transformer driving a unilateral amplifier and filter, for increased selectivity. See the LM2893-specific applications section.

For a LM1893-style transformer application, first, choose the turns ratio N based on an estimated lowest Z_L likely encountered, Z_{LN}. *Figure 29* shows graphically how N affects line signal. N should be as large as possible to drive Z_{LN} with full signal. If T_1 has an unloaded Q, Q_U, of well less than 35, a guess of N somewhat high should be used and later checked for accuracy. The recommended transformers have secondary taps giving a choice of N = 7.07, 10, and 14.1 (nominally) for driving Z_{LN}'s of 14, 7.0, and 3.5 Ω respectively (at $T_J = 25°C$, $V+ = 18V$, and $Q_U = 35$).

The resonating inductance of the tuned primary, L_1, is sought. Note that, while standard transformer design gives a transformer self-inductance with an impedance at operating frequency well above load impedance, the tuned transformer requires a low L_1 for adequate Q_U and minimum line pull. Result: relatively poor mutual coupling.

$$L_1 = \frac{R}{2\pi F_O Q} \tag{3}$$

It is known that resonant frequency $F_Q = F_O$ and some minimum bandwidth, or maximum Q, will be required to pass signal under full load conditions.

$$L_1 = \frac{R_Q \parallel |Z_{LN}|'}{2\pi F_O Q_L} \tag{4}$$

$|Z_{LN}|'$ is the reflected Z_{LN}, Q_L is the loaded Q, and parallel resistance R_Q models all transformer losses and sets Q_O.

$R_Q \parallel |Z_{LN}|'$ is found knowing that it absorbs full rated power.

The Coupling Transformer (Continued)

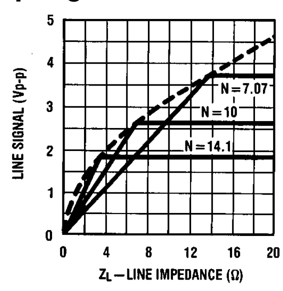


FIGURE 29. Impressed line voltage for a given Z_L for each of the 3 taps available on the recommended transformers

$$P_O = I_O V_O = \frac{I_{OPP}}{2\sqrt{2}}\left[\frac{2(-V_{ALC}+V_+)}{2\sqrt{2}}\right] = \frac{(-4.7+V_+)I_O}{4} \quad (5)$$

where I_O is in amps peak-to-peak at an elevated T_J

$$P_O = \frac{(18 - 4.7)\ 0.06}{4} = 0.200\ W \quad (6)$$

$$R_Q \| \, |Z_{LN}|' = \frac{V_O^2}{P_O} = \frac{(-V_{ALC} + V_+)\sqrt{2}}{I_O} = 442\ \Omega \quad (7)$$

R_Q is found using Z_{LN} and the value for N found when assuming $Q_U = 35$.

$$|Z_{LN}|' = N^2 Z_{LN} = (7.07)^2\ 13.9 = 695\ \Omega \quad (8)$$

$$R_Q = \frac{1}{\frac{1}{R_Q \| \, |Z_{LN}|'} - \frac{1}{|Z_{LN}|'}} = \frac{1}{\frac{1}{442} - \frac{1}{695}} = 1210\ \Omega \quad (9)$$

$$R_{QS} = \frac{R_Q}{1 + Q_U^2} = \frac{1210}{1 + 35^2} = 1\ \Omega \quad (10)$$

Only Q_L remains to be found to calculate L_1. Q_L is related to the −3 dB (half-power) bandwidth by

$$Q_L = \frac{1}{BW\ (\%\ of\ F_O)} \quad (11)$$

An iterative solution is forced where line pull, ΔF_Q, must be guessed to find Q_L and L_1. L_1 is then used to check the line pull guess; a large error requires a new guess. Try a BW of 8.7% - that is 4.4% for deviation, 1% for TC of F_O, and 3.3% for ΔF_Q - giving $Q_L = 11.5$.

$$L_1 = \frac{442}{2\pi \times 125\ 000 \times 11.5} = 49.0\ \mu H \quad (12)$$

Knowing the core inductance per turn, L, and L_1, the number of turns is found.

$$T_1 = \sqrt{\frac{L_1}{L}} = \sqrt{\frac{49.0\ \mu H}{20\ nH/T}} = 49\ 1/2\ turns \quad (13)$$

T is normally an integer, but these transformers require so few turns that half-turns are specified, remembering that the remaining ½ turn is completed on the P.C. board and is loosely coupled. The secondary turns are calculated

$$T_2 = \frac{T_1}{N} = \frac{49.5}{7.07} = 7.00 = 7\ turns \quad (15)$$

giving an L_2 of 0.98 μH. Note that the recommended 125 kHz transformer mirrors these specifications. The resonating capacitor is

$$C_Q = \frac{1}{(2\pi F_Q)^2\ L_1} = 33.1 \times 10^{-9} = 33\ nF \quad (16)$$

Line pull ΔF_Q was calculated (reference 3) for a Z_L magnitude of 14Ω and up with any phase angle from −90° to 90°. ΔF_Q was 6.4% - well above the 3.3% estimate. Referring to (11), an 11.8% bandwidth is required, forcing L_1 to be reduced to reduce Q. That fix was not implemented; some signal attenuation under worst-case drift and ΔF_Q is allowed. L_1 is already so small that the 31 gauge winding conducts a ¼ A_{RMS} circulating current.

Line Carrier Detection

While the addition of a carrier detection circuit (for a mute or squelch function) will only decrease receiver ultimate sensitivity, there is sometimes good reason to employ it to free the controller from watching for RX signal when no carrier is incoming, or to employ it to reduce the probability of line collisions (when multiple transmitters operate simultaneously to cause one or more transmissions to fail). Unless the detector is heavily filtered or uses a high carrier amplitude threshold, there will be false outputs that force the controller to have Data Out data checking capability just as is required when using no carrier detector. If false triggering is minimized, the probability of line collisions is increased due to the inability to sense low carrier amplitudes and because of sense delay. The property of the LM1893 to change output state infrequently (although the polarity is undefined) when in the RX mode, with no incoming carrier, reduces the desire to implement carrier detection and preserves the full ultimate sensitivity. Also, many impulse-noise insensitive transmission schemes, like handshaking, are easily modified to recover from line collisions.

Regarding this, it should be stated that for very complicated industrial systems with long signal runs and high line noise levels, it is probably wise to use a protocol which is inherently collision free so that no carrier detect hardware or software is needed. A token passing protocol is an example of such a system.

Figure 30 shows a low cost carrier amplitude detection circuit.

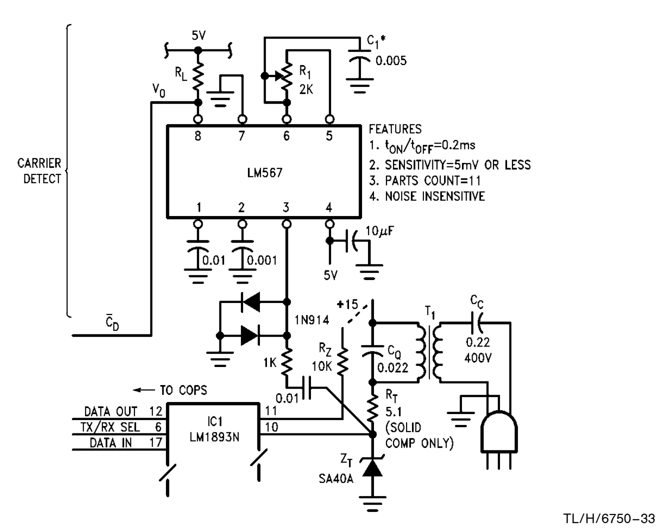
Audio Transmission

The LM1893 is designed to allow analog data transmission and reception. Base-band audio-bandwidth signals FM modulate the carrier passing through the tuned transformer (placing a limit on the usable percent modulation) onto the power line to be linearly demodulated by the receiver PLL. Because the receiver data path beyond the phase detector will pass only digital signal, external audio filtering and amplification is required. *Figure 31* shows a simple audio transmitter and receiver circuit utilizing a carrier detection mute circuit. A single LM339 quad. comparator may be used to build the carrier detect and mute. Filter bandwidth is held to a minimum to minimize noise, especially line-related correlated noise.

Communication and System Protocols

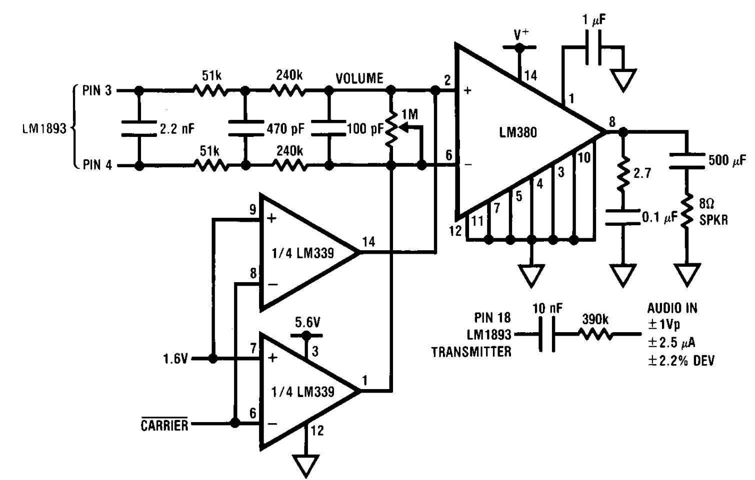
The development of communication and system protocols has historically been the single most time consuming element in design of carrier current systems. The protocols are defined as the following:

1. *Communication protocol*: a software method of encoding and decoding data that remains constant for every transmis-



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FIGURE 30. A simple carrier amplitude detector with output low when carrier is detected



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FIGURE 31. A simple linear analog audio transmitter and receiver are shown. The carrier and 1.6V inputs are derived from the carrier detector of *Figure 30*. The remaining 2 LM339 comparators may be used to build the carrier detector circuit.

Communication and System Protocols (Continued)

sion in a system. Its first purpose is to put data in a baseband digital form that is more easily recognized as a real message at the receive end. Secondly, it incorporates encoding techniques to ensure that noise induced errors do not easily occur; and when they do, they can always be detected. Lastly, the software algorithms that are used on the receive end to decode incoming data prevent the reception of noise induced ''phantom'' messages, and insure the recovery of real messages from an incoming bit stream that has been altered by noise.

2. *System protocol*: the manner in which messages are coordinated between nodes in a system. Its first purpose is to ensure message retransmission to correct errors (handshake). Secondly it coordinates messages for maximum utilization and efficiency on the network. Lastly, it ensures that messages do not collide on the network. Common system protocols include master-slave, carrier detect multiple access, and token passing. Token passing and master slave have been found to be the most useful since they are inherently collision free.

Both protocols usually reside as software in a single microcontroller that is connected to the LM1893/2893 I/O. In any case, some sort of intelligence is needed to process incoming and outgoing messages. UARTs have no usefulness in

Communication and System Protocols (Continued)

carrier current applications since they do not have the intelligence needed to distinguish between real messages and noise induced phantoms.

The difficulty in designing special protocols arises out of the special nature of the AC line, an environment laden with the worst imaginable noise conditions. The relatively low data rates possible over the AC line (typically less than 9600 baud) make it even more imperative that systems utilize the most sophisticated means available to ensure network efficiency.

With these facts in mind, the designer is referred to a publication intended to aid in the development of carrier current systems. This is literature #570075 The Bi-Line Carrier Current Networking System, a 200 pp. book that functions as the "bible" of Bi-Line system design. It has sections on LM1893 circuit optimization, protocol design, evaluation kit usage, critical component selection, and the Datachecker/DTS case study.

Basic Data Encoding (please refer to the previously mentioned publications for advanced techniques)

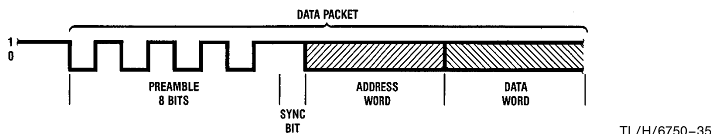
At the beginning of a received transmission, the first 0 to 2 bits may be lost while the chip's receiver settles to the DC bias point required for the given transmitter/receiver pair carrier frequency offset. With proper data encoding, dropped start bits can be tolerated and correct communication can take place. One simple data encoding scheme is now discussed.

Generally, a CCT system consists of many transceivers that normally listen to the line at all times (or during predetermined time windows), waiting for a transmission that directs one or more of the receivers to operate. If any receiver finds its address in the transmitted data packet, further action such as handshaking with the transmitter is initiated. The receiver might tell the transmitter, via retransmission, that it received this data, waiting for acknowledgement before acting on the received command. Error detecting and correcting codes may be employed throughout. The transmitter must have the capability to retransmit after a time if no response from the receiver is heard - under the assumption that the receiver didn't detect its address because of noise, or that the response was missed because of noise or a line collision. (A line collision happens when more than 1 transmitter operates at one time - causing one or more of the communications to fail). After many re-transmissions the transmitter might choose to give up. Collision recovery is achieved by waiting some variable amount of time before retransmission, using a random number of bits delay or a delay based on each transmitter's address, since each transceiver has a unique address.

An example of a simple transmission data packet is shown in *Figure 32*. The 8 bit 50% duty-cycle preamble is long enough to allow receiver biasing with enough bits left over to allow the receiver controller to detect the square-wave that signals the start of a transmission. If there had been no transmission for some time, the receiver would simply need to note that a data transition had occurred and begin its watch for a square-wave. If the receive controller detected the alternating-polarity data square-wave it would then use the sync. bit to signal that the address and data were immediately following. The address data would then be loaded, assuming the fixed format, and tested against its own. If the address was correct, the receiver would then load and store the data. If the address was not correct, either the transmission was not meant for this receiver or noise has fooled the receiver. In the former case, when the transmission was not meant for the receiver, the controller should immediately return to watching the incoming data for its address. If the later case were true, then the receive controller would continue to detect edges, tieing itself up by loading false data and being forced to handshake. The square-wave detection and address load and check routines should be fast to minimize the time spent in loops after being false-triggered by noise. If the controller detects an error (a received data bit that does not conform to the pre-defined encoding format) it should immediately resume watching the LM1893's Data Out for transmissions, the next bit would be shifted in and the process repeated.

A line-synchronous CCT system passing 3 bits per half-cycle may replace the long 8 bit preamble and sync pulse with a 2 bit start-of-transmission bias preamble. The receive controller might then assume that preamble always starts after bit 1 (the first bit after zero-crossing) so that any data transition at a zero crossing must be the start of the address bits and is tested as such. The line synchronous receiver operates with a simpler controller than an asynchronous system.

Discussion has assumed that the controller has always known when the Data Out is high or low. The controller must sample at the proper time to check the Data Out state. Since noise shows itself as pulse width jitter, symmetrically placed about the no-noise switch-points, optimum Data Out sampling is done in the center of the received data pulse. The receive data path has a time delay that, at low data rates, is dominated by the impulse noise filter integrator and is nominally ½ bit. At a 2 kHz data rate, an additional delay of approximately 1⁄10 bit is added because of the cumulative delay of the remainder of the receiver. *Figure 33* shows that Data Out sampling occurs conveniently at the transmitted



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FIGURE 32. A simple encoded data packet, generated by the transmit controller is shown. The horizontal axis is time where 1 bit time is $1/(2f_{DATA})$

Basic Data Encoding (Continued)

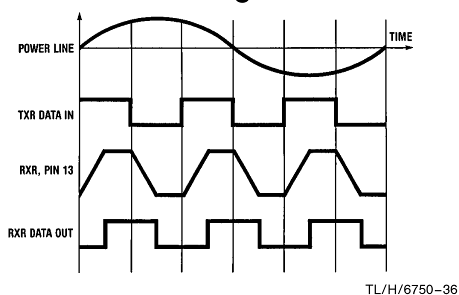


FIGURE 33. Operating waveforms of a line-synchronized transceiver pair are shown. The diagram shows how the transmitted data transitions may be used as received data sampling points

data edges for the line synchronous data transmission scheme mentioned in the previous paragraph. With the asynchronous system suggested, the receive controller must sample the Data Out pin often to determine, with several bits of accuracy, where the square-wave data transitions take place, average their positions assuming a known data rate, and calculate where the center of the data bits are and will continue to be as the address and data are read. A long preamble is helpful. Software that continuously updates the center-of-bit time estimate, as address and data are received, works even better. Alternatively, a coding scheme employing an embedded clock can be used.

LM2893 Application Hints

The LM2893 is intended for advanced applications where special circuitry is used in the transmit and receive paths. The LM2893 makes this possible by featuring separate transmit output and receive input pins.

Examples of enhancements that can be added to the basic LM1893/2893 circuit include separate transmit and receive windings on the coupling transformer, high quality ceramic or LC filters in the receive path, and simple impulse noise blanking circuits.

In many applications, the additional performance to be gained outweighs the extra cost of the additional circuitry. More than likely, high performance industrial applications such as building energy management will fit into this category, since they require the utmost in reliability.

Because of the specialized nature of individual LM2893 applications, it is not possible to give one circuit that will satisfy all requirements for performance and cost effectiveness. Therefore no specific application examples will be given. Instead the subsequent text describes in general terms the types of circuits that can be used to increase performance along with their advantages and disadvantages. It is intended to be a springboard for ideas.

LM2893 COUPLING NETWORKS

The main disadvantages of the typical LM1893 coupling network are that it functions as the bandpass filter, has loose coupling between primary and secondary, and has a single secondary. The LM1893 coupling network was designed this way mainly because of the restraint that the carrier input and output are tied together.

Because the coupling transformer is used as a filter, the LM1893 circuit is susceptible to pulling of the center frequency under conditions of changing line impedances or when several LM1893 circuits are close in proximity on the AC line. Because the tuned transformer has a high value of "Q", ringing also occurs in the presence of impulsive noise. This ringing occurs at the center frequency and increases the error rate of transmissions, especially at relatively high data rates (>2000 baud). Because it is the only tuned circuit in the system, the selectivity characteristics leave a lot to be desired.

The LM2893, having separate receive input and transmit output pins, removes the limitations on coupling transformer design, allowing the design of circuits devoid of the previous limitations.

The first enhancement that can be made with the LM2893 circuit is the use of a high permeability ferrite toroid for line coupling along with a separate filter. The transformer would be of broadband design (untuned) with two secondaries, one for coupling to the transmit output and one for coupling to the receive input. This allows impedance matching of both the transmitter and receiver, with the result of quite a bit more receive sensitivity.

Because of the increased signal and separate receive signal path, a 3 or 6 db pad can be used before the selective stages to eliminate pulling of the center frequency due to changes in line impedance.

Another advantage of the toroidal transformer is that it can be designed for use at very low line impedances due to its inherent tight coupling.

SEPARATE FILTER

Because of the separate receive path of the LM2893, a relatively high quality bandpass filter can be used for selectivity. Inexpensive ceramic filters are available that have bandpass and center frequency characteristics compatible with carrier current operation. Futhermore, the use of these filters allows multichannel operation, previously made difficult by the single tuned network of the LM1893. These filters are easily cascaded for even more off-frequency rejection. If the pad is added before the filter, there will be negligible pulling due to changes in line impedance reflected through the coupling transformer.

Alternatively, a Butterworth/Chebyshev bandpass LC filter or an active filter can be used in place of the ceramic filter.

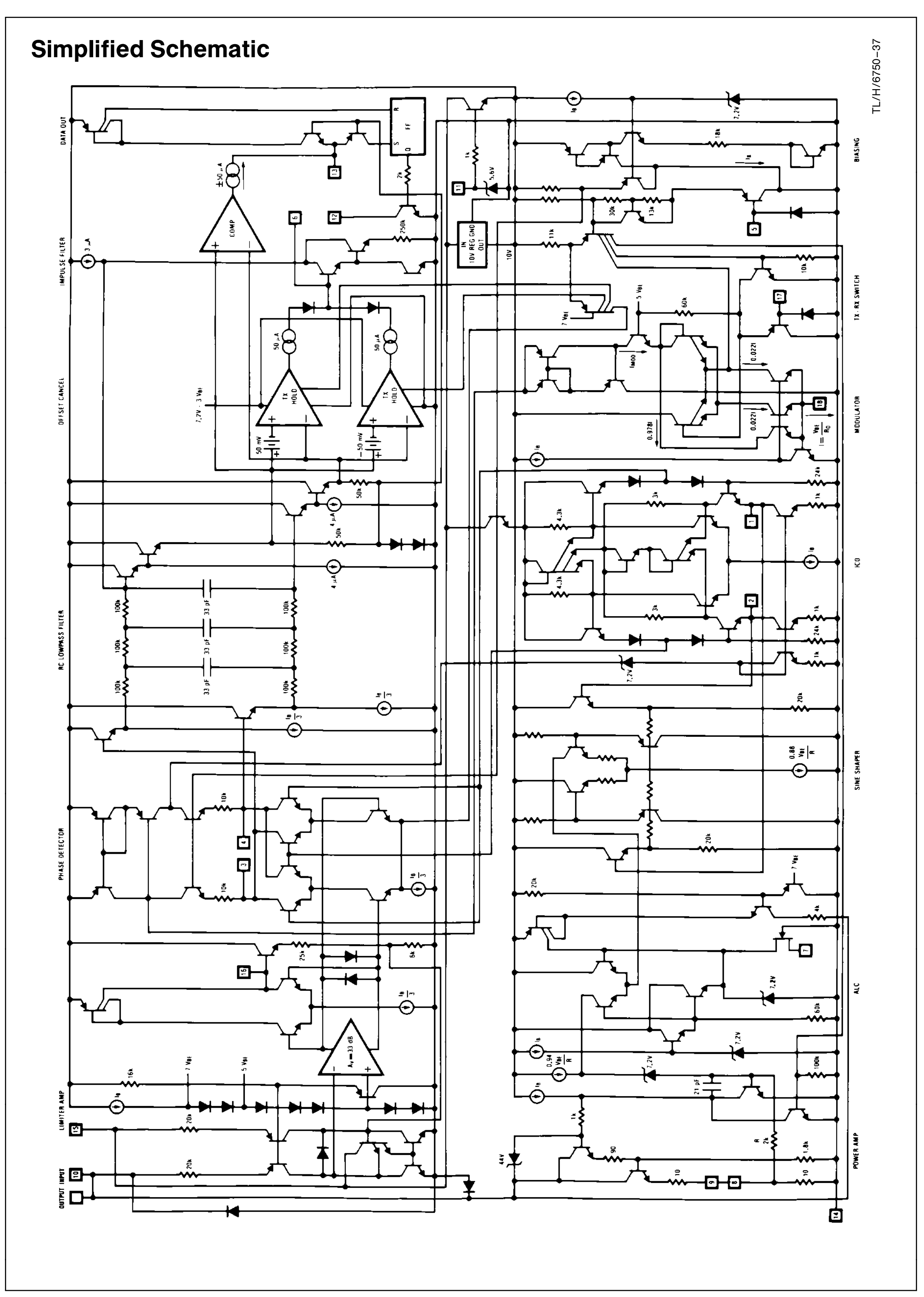
IMPULSE NOISE BLANKER

Although the LM2893 has adequate impulse noise rejection for most applications, there is reason to employ impulse blanking to improve error rates in severe AC line environments. Typically, errors occur due to pulse jitter in the LM1893/2893 data output that originates when the internal time domain filter smooths out an incoming noise pulse.

The solution involves removing the impulse completely and not simply trying to filter it. Moreover, the pulse should be removed in the receive signal path before the selective portions of the circuit to eliminate ringing. This also allows the receiver filter to smooth out the blanks that also occur in the desired incoming carrier signal.

If a carrier detect circuit is desired in conjunction with the LM2893 it can be located after the filter and impulse blanker. Because impulse noise is removed, the false triggering that plagues these circuits will be greatly reduced.

Simplified Schematic

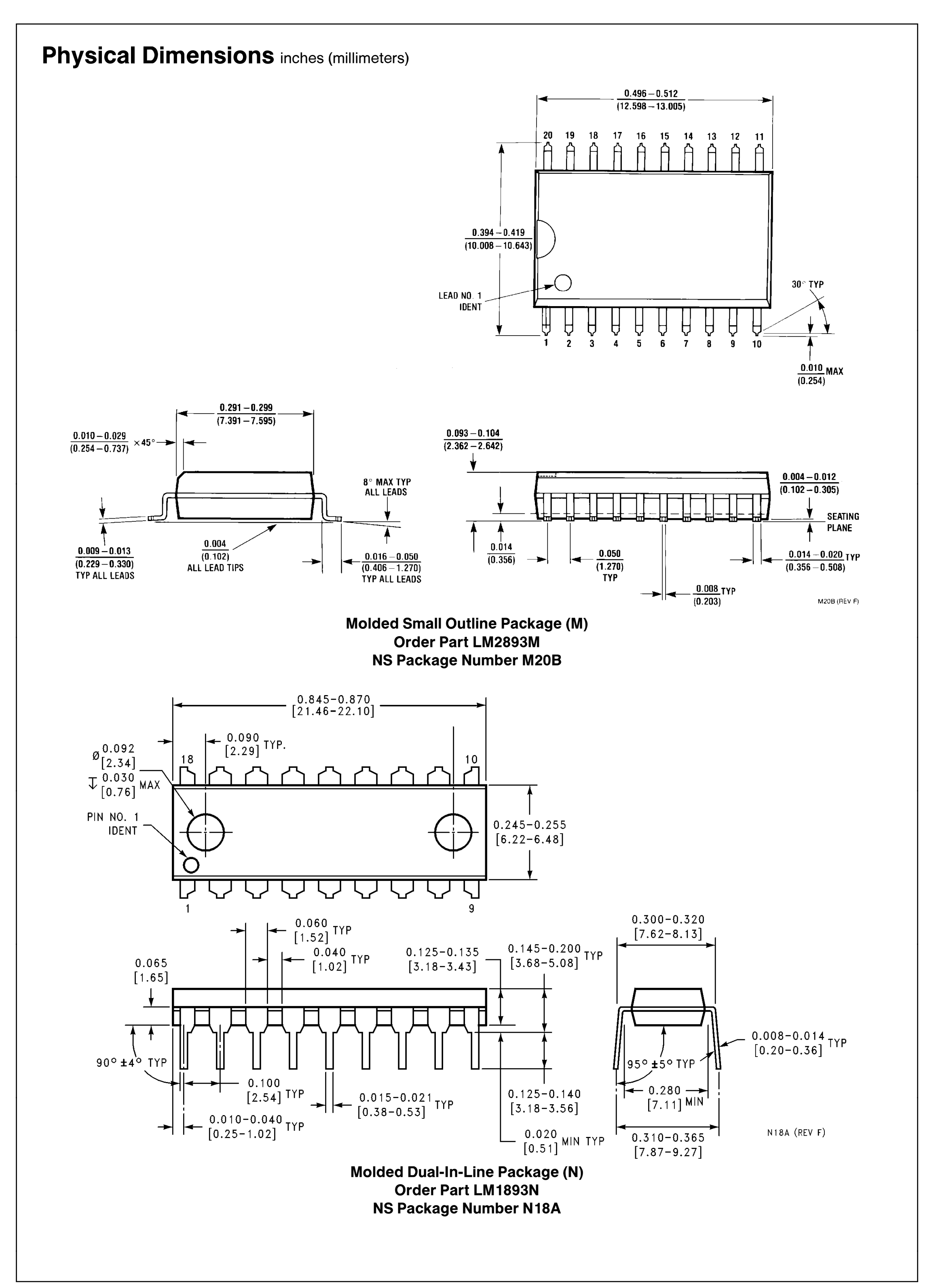


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References

1. Nicholson, J.R. and J.A. Malack; ''RF Impedance of Power Lines and Line Impedance Stabilization Network in Conducted Interference Measurements;'' IEEE Transactions on Electromagnetic Compatibility; May 1973; (line impedance data)
2. Southwick, R.A.; ''Impedance Characteristics of Single-Phase Power Lines;'' Conference Rec.; 1973 IEEE Int. Symp. on Electromagnetic Compatibility; (line impedance data)
3. Hayt, William H. Jr. and Jack E. Kemmerly; ''Engineering Circuit Analysis;'' McGraw-Hill Books; 1971; pp. 447–453; (linear transformer reflected impedance)
4. FCC, ''Notice of Proposed Rule Making,'' Docket 20780, adopted Apr. 14, 1976, (Proposed regulation)
5. Monticelli, Dennis M. and Michael E. Wright; ''A Carrier Current Transceiver IC for Data Transmission Over the AC Power Lines;'' IEEE J. Solid-State Circuits; vol. SC-17; Dec. 1982; pp. 1158-1165; (LM1893 circuit description)
6. Lee, Mitchell; ''A New Carrier Current Transceiver IC;'' IEEE Trans. on Consumer Electronics; vol. CE-28; Aug. 1982; pp. 409–414; (Application of LM1893)

Physical Dimensions inches (millimeters)

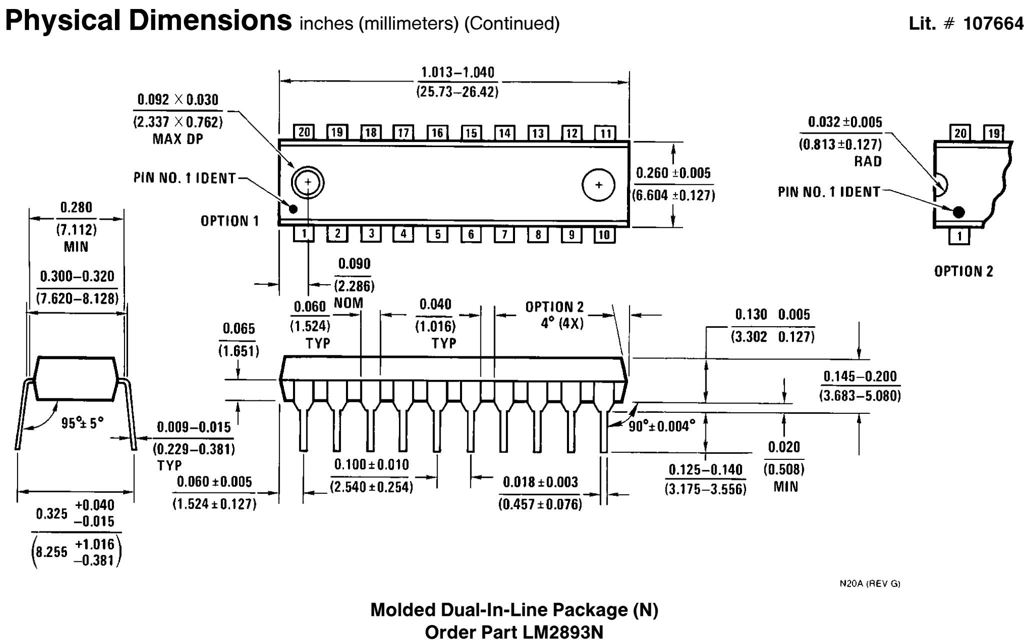


Molded Small Outline Package (M)
Order Part LM2893M
NS Package Number M20B

Molded Dual-In-Line Package (N)
Order Part LM1893N
NS Package Number N18A

Physical Dimensions inches (millimeters) (Continued)

Lit. # 107664



Molded Dual-In-Line Package (N)
Order Part LM2893N
NS Package Number N20A



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